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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S)	:	Dale T. Platteter, et al.
TITLE	:	SYSTEM ARCHITECTURE AND METHOD FOR SYNCHRONIZATION OF REAL-TIME CLOCKS IN A DOCUMENT PROCESSING SYSTEM
APPLICATION NO.	:	09/938,237
FILED	:	August 23, 2001
CONFIRMATION NO.	:	1618
EXAMINER	:	Tse W. Chen
ART UNIT	:	2116
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TRANSMITTAL OF
REPLY BRIEF UNDER 37 C.F.R. 41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant transmits herewith one (1) copy of REPLY BRIEF UNDER 37 C.F.R. 41.41 for the above-reference patent application.

The commissioner is authorized to charge Deposit Account No. 24-0037 for any fee deficiency.

Respectfully submitted,

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Date: 9/6/05

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I hereby certify that this Transmittal of Reply Brief Under 37 C.F.R. 41.41 is being sent by the United States Postal Service as Express Mail procedure and is addressed to Mail Stop – Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. **Express Mail No. EV 702958757 US**

Elaine M. Checovich

Date: 9-6-05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Dale T. Platteter, et al.

Application No.: 09/938,237 Examiner: Tse W. Chen

Filed: August 23, 2001 Docket No.: A0A73-US-NP
XERZ 2 00424

For: SYSTEM ARCHITECTURE AND METHOD FOR SYNCHRONIZATION OF REAL-TIME CLOCKS IN A DOCUMENT PROCESSING SYSTEM

APPELLANTS' REPLY BRIEF UNDER 37 CFR 41.41

Appeal from Group 2116

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A. Preliminary Matters

At the outset, appellants respectfully submit that certain comments they made in the Appeal Brief do not constitute "admissions" as suggested by the Examiner throughout the Answer (see, for example, Examiner's Answer, pages 14, 16, 17, 18, 20, 23). Rather, appellants' statements simply constitute a reiteration of statements made by the Examiner during prosecution of the application, *i.e.*, background information. The Examiner's mischaracterization of these statements in the Appeal Brief is misleading and incorrect.

B. The Examiner Failed to Establish Any Suggestion or Motivation to Combine Miyawaki and Yamanaka

Appellants use a discrete hardware interrupt signal between modules that reside on a network to remove any inherent network communications delay. Appellants then use the network to communicate the time at which the interrupt was generated to synchronize the clocks between the modules. Not one of the cited patents relates to this novel concept. And it is not possible to obtain this concept even if all of the cited patents are combined.

For example, claims 1 and 21 of the application include "a master clock and logic for generating a discrete clock synchronization interrupt signal." Likewise, claims 13 and 15 include "generating a discrete clock synchronization interrupt signal in the control and distributing the clock synchronization interrupt signal to the resource via the control bus." On the other hand, Yamanaka (U.S. Pat. No. 4,807,259) is a solution based solely upon a *serial communications channel.* Yamanaka measures the round trip delay and attempts to adjust for the delay. However, such delay is not symmetrical or consistent. Thus, there will be inherent inaccuracies based upon the amount of message traffic on the serial communications channel. This differs from claim one which includes a *discrete*

signal that all the processors receive simultaneously. This feature removes the delay and consequently any notion of having to adjust for it. Obviously, this is much more accurate but admittedly comes at the expense of an extra wire connecting processors. This is perfectly fine for appellants' environment as the modules that contain these processors are physically located close to each other. Of course, it would be more difficult to apply this approach to processors that were widely distributed, as in separate buildings or states.

Likewise, Miyawaki (U.S. Pat. No. 5,995,771) has nothing to do with clock synchronization nor is it ever mentioned in that patent. FIG. 3 suggests that there is an interrupt signal between a CPU and a copy controller but it is not discussed in the specification. It is not even numbered such that it could be referred to in the document. It is apparently nothing more than an interrupt signal between processors contained on the same printed wiring board. As known to those skilled in the art, this is extremely common in the electronics industry and one would be hard pressed to find a CPU that does not have some kind of interrupt wired to it. Again, this signal does not connect modules and Miyawaki does not even mention synchronization of clocks. It does discuss an image forming apparatus, but that is where the similarities end. Miyawaki most closely refers to a concept known as cluster printing, where the user may utilize multiple printers to schedule a job to and then pick the most available printer within a cluster of printers. Miyawaki does connect the "service terminal" to the printers (*i.e.*, copiers) via a LAN but that is where the similarities end.

The Examiner has also asserted that it would have been obvious to combine certain aspects of Yamanaka with Miyawaki to produce the claimed invention. However, the Examiner has provided no reference or other evidence to support the

conclusion that it would be obvious to one skilled in the art to modify the processing system of Miyawaki with the teachings of Yamanaka, aside from conclusory statements such as these: "It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the synchronization teachings of Yamanaka into the document processing system of Miyawaki in order to synchronize operations among the resources and controller of the marking engine. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use." (See page 8 of the Office Action mailed 11/30/2004.)

A *prima facie* case of obviousness is not established absent proper motivation. Simply because certain teachings of Yamanaka *could* be misconstrued and then used in certain document processing systems, a motivation to modify Miyawaki to meet the limitations of the claims is not formed. Moreover, according to MPEP §2144.01, the "fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness." Merely because the claimed elements are individually found in the prior art, it does not necessarily follow that it would be obvious to combine the elements from different prior art references. *See* MPEP §2141.01, citing *Ex Parte Levingood*, 28 USPQ2d 1300 (Bd. App. 1993).

Consequently, absent a motivation to combine and modify Miyawaki with the teachings of Yamanaka, it is irrevelent that the elements and/or limitations may be individually or separately known in the prior art. Clearly, the Examiner was motivated to combine these teachings for no other reason than to arrive at the claimed invention. This is a classic example of impermissible hindsight.

Granted, the Examiner's function is a difficult one. However, the standards for examining patents must not be compromised by affirming Section 103 rejections reached in this manner. The Court of Appeals for the Federal Circuit has recognized this danger and explained: "Our case law makes clear that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references." *Ecolochem, Inc. v. Southern California Edison Co.,* 227 F.3d 1361, 1371, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000); "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

So, the Federal Circuit demands that there be a showing of the teaching or motivation to combine the references. To dispel any issue concerning this requirement, the Federal Circuit has unambiguously stated, "[w]hen relying on numerous references or a modification of prior art, it is incumbent upon the examiner to identify some suggestion to combine references or make the modification." *In re Mayne*, 104 F.3d 1339, 1342, 41 USPQ2d 1451, 1454 (Fed. Cir. 1997).

In the present case, the Examiner has not identified any suggestion or motivation for combining the teachings of Miyawaki (the primary reference) with the teachings of Yamanaka (the secondary reference). This is a fatally deficient flaw in reaching the rejection under § 103. This is one of several reasons why the present rejection must be reversed.

C. CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-21 are in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the rejections of claims 1-21.

Respectfully submitted,

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I certify that Appellants' Reply Brief Under 37 CFR 41.41 is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated below and is addressed to Mail Stop Appeal Brief - Patents Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313 -1450.	
Express Mail Label No.: EV 702958757 US	**Signature** Elaine M. Checovich
Date 9-6-05	**Printed Name** Elaine M. Checovich